Patent claims

1. An integrated read-only memory,
   - having selection transistors each having a drain connection,
   - having an electrode for feeding a voltage or a current,
   - having a layer between the drain connections and the electrode, the electrical resistance of which can be changed through the effect of a configuration voltage or a configuration current.

2. The read-only memory as claimed in claim 1,
   - in which the layer is formed as a common layer for linking the drain connections to the electrode, and
   - in which the electrical resistance of the layer can be changed locally.

3. The read-only memory as claimed in claim 1 or claim 2, in which the resistance of the layer can be switched over.

4. The read-only memory as claimed in one of the preceding claims, in which the resistance of the layer can be switched over between two resistance characteristic curves.

5. The read-only memory as claimed in one of the preceding claims,
   - having a read voltage applied to the layer or a read current fed to the layer within a defined voltage or current range in a read operation of the read-only memory, and
   - having a configuration voltage or a configuration current outside the voltage or current range provided for the read operation in a configuration operation of the read-only memory.

6. The read-only memory as claimed in one of the preceding claims, which is designed as a flash memory.

7. The read-only memory as claimed in one of the preceding claims, in which the selection transistors are arranged in an array.

8. The read-only memory as claimed in one of the preceding claims,

- having a source connection per selection transistor, and
- having a bit line that is electrically connected to at least one source connection.

9. The read-only memory as claimed in claim 8, in which the bit line is connected to a decoder circuit.

10. The read-only memory as claimed in claim 8 or claim 9, in which the bit line is accessible for an external connection.

11. The read-only memory as claimed in one of the preceding claims,

- having a gate connection per selection transistor, and
- having a word line that is electrically connected to at least one gate connection.

12. The read-only memory as claimed in claim 11, in which the word line is connected to a decoder circuit.

13. The read-only memory as claimed in claim 11 or claim 12, in which the word line is accessible for an external connection.

14. The read-only memory as claimed in one of the preceding claims, in which the selection transistors have a planar construction in the substrate.

15. The read-only memory as claimed in one of claims 1 to 13, in which the selection transistors have a vertical construction in the substrate.

16. The read-only memory as claimed in one of the preceding claims, in which the layer is formed as a molecular layer.

17. The read-only memory as claimed in claim 16, in which the layer contains rotaxane.

18. The read-only memory as claimed in claim 16, in which the layer contains catenane.

19. The read-only memory as claimed in claim 16, in which the layer contains a bispyridinium compound.

20. The read-only memory as claimed in one of claims 1 to 15, in which the layer is formed as a dielectric.

21. The read-only memory as claimed in claim 20, in which the layer contains $SrZrO_3$.

22. The read-only memory as claimed in one of claims 1 to 15, in which the layer is formed as a polymer.

23. The read-only memory as claimed in claim 22, in which the layer contains 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

24. The read-only memory as claimed in claim 22, in which the layer contains a chalcogenide compound.

25. A method for operating an integrated read-only memory as claimed in one of the preceding claims,

- in which in a read operation, a read voltage or a read current within a defined voltage or current range is applied to the layer, and
- in which, in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read operation is applied to the layer.

26. A method for producing an integrated read-only memory,

- in which an array of selection transistors is produced using CMOS technology,
- in which drain contacts of the selection transistors are led to the surface of the arrangement,
- in which a layer is deposited whose electrical resistance can be changed through the effect of a configuration voltage or a configuration current,
- in which an electrode is arranged above the layer.

27. The method for producing an integrated read-only memory as claimed in claim 26, in which the layer is deposited as a common layer for linking the drain connections to the electrode above the selection transistors.

28. The method for producing an integrated read-only memory as claimed in claim 26 or claim 27, in which the selection transistors are produced in a front end process.

29. The method for producing an integrated read-only memory as claimed in one of claims 26 to 28, in which the layer is deposited in a back end process.

30. The method for producing an integrated read-only memory as claimed in one of claims 26 to 29, in which the selection transistors are constructed in planar fashion in the substrate.

31. The method for producing an integrated read-only memory as claimed in one of claims 26 to 29, in which the selection transistors are constructed vertically in the substrate.

32. The method for producing an integrated read-only memory as claimed in one of claims 26 to 31, in which the layer is formed as a molecular layer.

33. The method for producing an integrated read-only memory as claimed in claim 32, in which the layer contains rotaxane.

34. The method for producing an integrated read-only memory as claimed in claim 32, in which the layer contains catenane.

35. The method for producing an integrated read-only memory as claimed in claim 32, in which the layer contains a bispyridinium compound.

36. The method for producing an integrated read-only memory as claimed in one of claims 26 to 31, in which the layer is formed as a dielectric.

37. The method for producing an integrated read-only memory as claimed in claim 36, in which the layer contains $SrZrO_3$.

38. The method for producing an integrated read-only memory as claimed in one of claims 26 to 31, in which the layer is formed as a polymer.

39. The method for producing an integrated read-only memory as claimed in claim 38, in which the layer contains a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

40. The method for producing an integrated read-only memory as claimed in one of claims 26 to 31, in which the layer contains a chalcogenide compound.